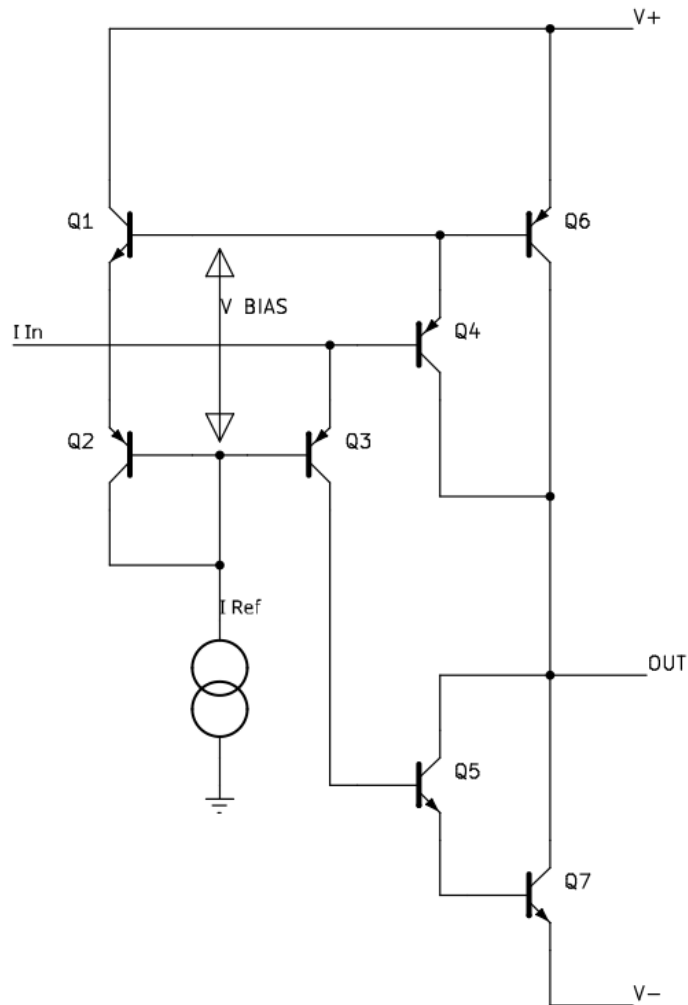


Non-switching Class AB design

The schematic below partly shows the design by Jager et al. [1] to realize a non-switching class AB output stage. The control current from the input stage is called I_{In} . The output (OUT) is taken from the Darlington output transistors Q_4/Q_6 and Q_5/Q_7 . The power transistors are Q_6 and Q_7 , while the drivers are Q_4 and Q_5 . Please notice that these transistors operate in common emitter configuration. This implies that the open loop output impedance is quite high, demanding a fair amount of open loop gain to realize a closed loop low output impedance. The control loop is realized by the transistors Q_1 - Q_4 .



It is seen that:

$$V_{BIAS} = V_{BE1} + V_{BE2} = V_{BE3} + V_{BE4} \quad (1)$$

In general we have (Ebers-Moll, approximately):

$$I_C = I_S e^{V_{BE}/V_T} \quad (2)$$

where:

I_C : Collector current

V_{BE} : Base-emitter voltage

I_S : Leakage current

V_T : Thermal voltage, $V_T = kT/e$

k : Boltzmann constant: $1.3806 \cdot 10^{-23}$ J/K

T : Absolute temperature [K]

e : Elementary charge: $1.602 \cdot 10^{-19}$ C

From eq. 2, we then have:

$$V_{BE} = V_T \ln \frac{I_C}{I_S} \quad (3)$$

From eq.1 and 3, we can then exploit:

$$V_{BIAS} = V_T \ln \frac{I_{C1}}{I_S} + V_T \ln \frac{I_{C2}}{I_S} = V_T \ln \frac{I_{C3}}{I_S} + V_T \ln \frac{I_{C4}}{I_S} \quad (4)$$

Since approximately $I_{C1} = I_{C2} = I_{Ref}$, this leads to:

$$V_{BIAS} = V_T \ln \frac{I_{Ref}^2}{I_S^2} = V_T \ln \frac{I_{C3} \cdot I_{C4}}{I_S^2} \quad (5)$$

which leads to the expression:

$$I_{Ref}^2 = I_{C3} \cdot I_{C4} \quad (6)$$

We can assume that:

$$I_{C4} = I_{C5} = h_{FE} I_{C3} \quad (7)$$

where h_{FE} is the transistor current gain, assumed the same for all the transistors. Combining eq. 6 and 7, then gives:

$$I_{C4}^2 = h_{FE} \cdot I_{Ref}^2 \Rightarrow I_{C4} = I_{C5} = I_{Ref} \sqrt{h_{FE}} \quad (8)$$

It is seen that the function of Q_1 is to isolate Q_6 from the control loop, thus avoiding thermal runaway and switching distortion.

The current gain I_{OUT}/I_{In} for the output stage is approximately given by:

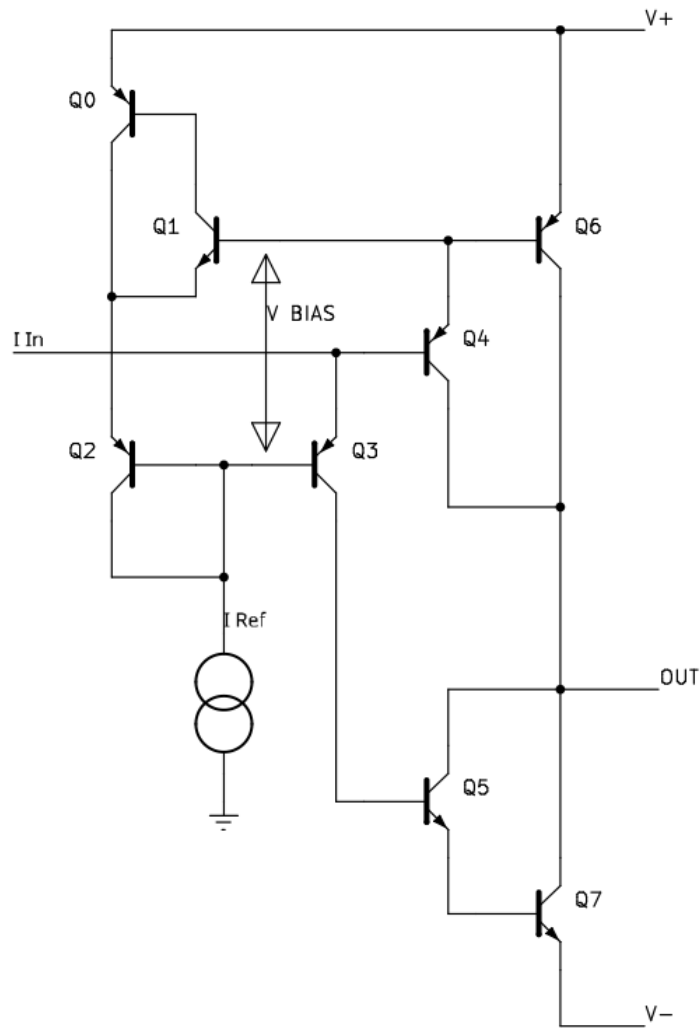
$$A_1 = h_{FE}^2 \quad (9)$$

The control loop can be optimised by adding another transistor Q_0 as shown in the figure below. Now the collector current of Q_1 is reduced with the current gain h_{FE} . So inserting $I_{Ref} = I_{C2} = h_{FE} I_{C1}$ into eq. 4, we have:

$$V_{BIAS} = V_T \ln \frac{I_{Ref}}{h_{FE} \cdot I_S} + V_T \ln \frac{I_{Ref}}{I_S} = V_T \ln \frac{I_{C3}}{I_S} + V_T \ln \frac{I_{C4}}{I_S} \quad (10)$$

This leads to:

$$\frac{I_{Ref}^2}{h_{FE}} = I_{C3} \cdot I_{C4} \quad (11)$$



Using eq. 7, we can write:

$$\frac{I_{Ref}^2}{h_{FE}} = I_{C3} \cdot I_{C4} = \frac{I_{C4}}{h_{FE}} \cdot I_{C4} \quad (12)$$

Then we have the expression (compare to eq. 8):

$$I_{C4} = I_{C5} = I_{Ref} \quad (13)$$

As a result the bias current of the power transistors now is given by:

$$I_{C6} = I_{C7} = h_{FE} \cdot I_{Ref} \quad (14)$$

The control loop now controls the bias current of the driver transistors directly with the means of the reference current I_{Ref} .

Reference:

1. Wim de Jager, Erik van der Ven and Ed van Tuyl: A new Class-AB design, Electronics World December 1999.

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